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# BANDWIDTH ENHANCEMENT IN DOHERTY POWER AMPLIFIERS: A COMPARISON OF CONVENTIONAL AND INVERTED ARCHITECTURES

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## ABSTRACT

Conventional Doherty power amplifiers (DPAs) face bandwidth issues due to poor impedance matching and input phase design. This paper explores ways to enhance DPA performance in frequency response. The study focuses on optimizing output matching network parameters and the input phase slope between main and auxiliary amplifiers to improve bandwidth efficiency, especially for mobile wireless applications.We calculate the voltage standing wave ratio (VSWR) for each DPA amplification stage at different power levels using MATLAB. We examine conventional and inverted DPA configurations at 2.5 GHz within the 2 GHz to 3 GHz range, utilizing an NXP GaN-based FET transistor model. The two-stage architectures include main amplifiers in Class B and auxiliary in Class C modes, analyzed at peak and back-off levels. Our results indicate that the inverted Doherty amplifier achieves a 40% fractional bandwidth compared to the 8% of the conventional DPA at a VSWR of 1.2, showing better performance due to greater parameter flexibility. These findings are significant for improving RF efficiency in 5G base stations and future wireless networks.

**Keywords**: Doherty Power Amplifier, Voltage standing wave ratio, Quarter-wave transmission line, Fractional bandwidth

## INTRODUCTION

The high-efficiency Doherty RF power amplifier (DPA) is named after engineer William H. Doherty, who invented it in 1936 while working at Bell Telephone Laboratories. His innovation aimed to improve high-power radio transmitters for both terrestrial and transoceanic broadcasting and telephony. Doherty amplifiers were later adapted for use with solid-state technology, marking a significant advancement in amplifier design (Saeedah, M.S. et al., 2023; Abubakar, N., 2023; Gareth, L., 2019; Frederick H.R., 1987; William H.D., 1936).

With the emergence of digital cellular radio systems in the late 1990s, interest in Doherty amplifiers revived to increase the electrical efficiency of base station transmitters. DPAs have since been extensively studied and employed to amplify multicarrier signals characterized by a high Peak-to-Average Power Ratio (PAPR). One of the main reasons for their popularity is their ability to maintain energy efficiency without complex control circuits. The Doherty technique allows power amplifiers to sustain efficiency across a range of input and output power levels (Nicolas et al., 2002; Abbas et al., 2021; Kerherve, 2005; Byung et al., 2010; Mehran, 2016; Masahiro et al., 2001).

The growing demand for high-data-rate wireless communication systems has increased the need for power-efficient and wideband RF power amplifiers. Doherty Power Amplifiers are widely adopted in modern wireless transmitters because they enhance efficiency at back-off power levels. However, conventional DPAs face bandwidth limitations due to impedance mismatch, phase dispersion, and the narrowband behaviour of the load modulation network. To overcome these challenges, researchers have explored alternative architectures, including the Inverted Doherty Power Amplifier (IDPA) architecture, which modifies the impedance transformation network to improve bandwidth performance (Amit Kumar et al., 2022; Jawad et al., 2010; Daehyun et al., 2011; Gustafsson, 2014; Gholamreza & Anding, 2019). Recent studies have emphasized the importance of optimizing input group delay to enhance bandwidth performance in Doherty power amplifiers beyond 40% (Cavarroc et al., 2023).

This paper analyzes the frequency behaviour of both conventional and inverted DPAs. We derive formulas to calculate the output network parameters as functions of frequency. Then, we optimize these parameters and the input phase slope between the main and auxiliary amplifiers of the DPA using the fmincon optimization function in MATLAB. Through this analysis, we aim to improve the bandwidth performance of DPAs while preserving efficiency, thereby contributing to the advancement of high-efficiency RF power amplification.

## MATERIALS AND METHODS

### Frequency behaviour of the conventional DPA

Figure 1 illustrates the schematic diagram of the conventional Doherty Power Amplifier (DPA). This circuit comprises a single quarter-wave transmission line at the output of the main amplifier, which presents an impedance of $Z_{CN}$ to the common node. At low output power levels, when the auxiliary amplifier is turned off, the load circuit of the main amplifier consists of two quarter-wave transmission lines (two $\lambda/4$ lines). When peak output power is reached, the auxiliary power amplifier is activated, serving as an active load for the main amplifier (Abdoul-Aziz, A.A., et al., 2024; Abbas, N., et al., 2022). The impedance notations at the outputs of both amplifiers and the two quarter-wave transmission lines are indicated.

In a two-stage symmetrical Doherty power amplifier configuration, the output currents of both amplifiers are equal at peak output power, which corresponds to a current ratio of |r| = 1. From the analysis of the circuit depicted in Figure 1 at the center frequency, $f_o$, we can derive the following expressions for the impedances to be used (Eric Kerherve, 2005; Mingzhe et al., 2020; W.C. Edmund Neo et al., 2007; James et al., 2018):

$Z_{C1} = Ropt$; $Z_{CN} = Ropt/2$; $Z_{C4} = \sqrt{50.Z_{CN}}$ (1)

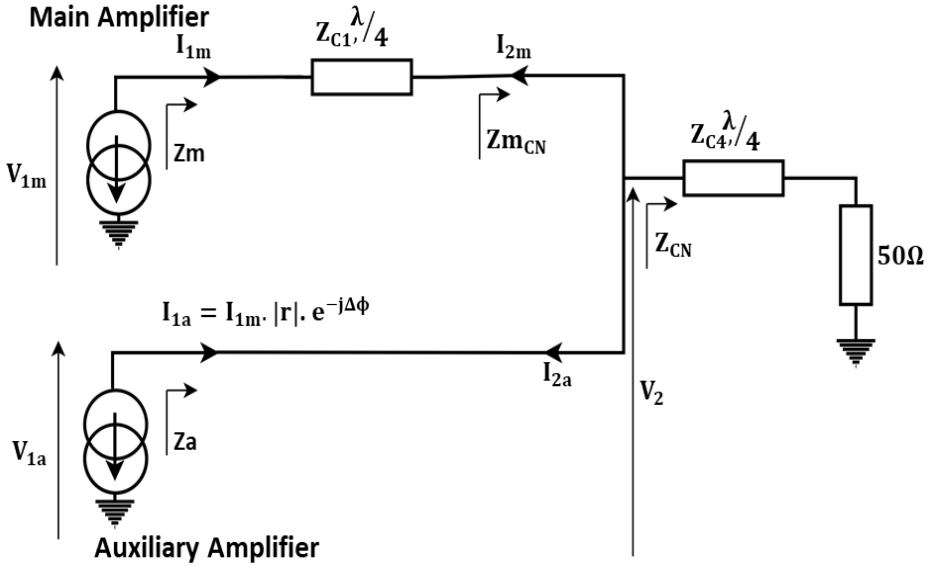


Figure 1: Block diagram of the conventional two-stage DPA architecture

The main and auxiliary power amplifier currents are represented by $I_{1m}$ and $I_{1a}$ respectively. From Figure 1, the expression for the complex ratio of the auxiliary to main amplifier current sources is given as:

$$r = \frac{I_{1a}}{I_{1m}} = |r|.e^{-j\Delta\phi} \quad (2)$$

The term "$\Delta\phi$", represents the phase difference between the two currents, which varies with frequency depending on the DPA circuit topology used. Thus, the expression for the phase difference as a function of radian frequency can be written in general form as:

$$\Delta\phi = \frac{\pi}{2} - \Delta\tau_{gd}.(\omega - \omega_o) \quad (3)$$

For $\omega = \omega_o$, the optimum phase value is equal to $\Delta\phi = \frac{\pi}{2}$, and $\Delta\tau_{gd}$ is the group delay expressed as:

$$\Delta\tau_{gd} = \frac{1}{\gamma.2f_o} \quad (4)$$

The following conditions can be defined for conventional DPA:

When an ideal phase shifter or a hybrid coupler is used in the Doherty circuit, the phase difference $\Delta\phi$ is constant and equal to $\Delta\phi = \frac{\pi}{2}$, as such, the group delay in this case, becomes: $\Delta\tau_{gd} = 0$.

When a quarter-wave transmission line is used, the phase difference is given by: $\Delta\phi = -\beta l = -\frac{\pi}{2}.\frac{\omega}{\omega_o}$. Hence, the group delay in this case becomes:

$\Delta\tau_{gd} = \frac{1}{\gamma.2f_o}$, and at $\gamma = 2$, the group delay is $\Delta\tau_{gd} = \frac{\pi}{2f_o}$

Other values of the input phase difference $\Delta\phi$ and phase slope parameter ($\gamma$) are obtained using a phase shifter circuit developed by (Manuel et al., 2023) based on the bandpass filter synthesis theory.

For the frequency study, the impedance expressions at the outputs of the main and auxiliary amplifiers are derived by modelling the two quarter-wave transmission lines in the conventional DPA circuit using a transmission matrix. The equations that describe the frequency behaviour of the conventional DPA are as given follows:

The ABCD transmission matrix enables the analysis of the frequency behaviour of a Doherty Power Amplifier (DPA). For instance, it simplifies the calculation of the input impedance ($Z_{in}$) of a quadripole with a loaded output impedance ($Z_{out}$), as illustrated in Figure 2.

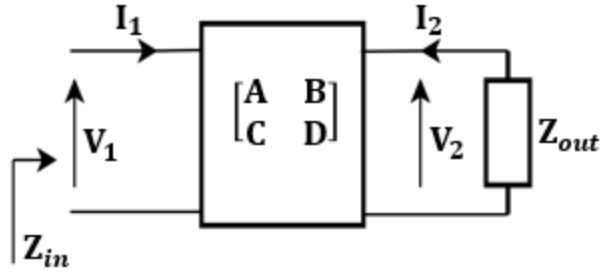


Figure 2: The calculation of input impedance ($Z_{in}$) of a quadripole loaded with ($Z_{out}$) with transmission matrix

The input variables of the quadripole shown in Figure 2 are given by the following equations:

$$\begin{cases} V_1 = A.V_2 - B.I_2 \\ I_1 = C.V_2 - D.I_2 \end{cases} \quad (5)$$

Thus, the input impedance Zin is obtained from equation (5) as the ratio of $V_1/I_1$.

$$Zin = \frac{A.Zout+B}{C.Zout+D} \quad (6)$$

with:

$$\text{Zout} = -\frac{V_2}{I_2} \quad (7)$$

With the auxiliary amplifier switched off at the back-off power level, the analysis of the conventional DPA circuit in Figure 1 is simplified. Thus, the load section of the circuit now consists of only the quarter-wave transmission line at the output of the main amplifier modelled as the quadripole matrix [Am Bm Cm Dm] and cascaded with the quadripole matrix [ABCD] of the output quarter-wave transmission line. Therefore, the impedance presented at the output of the main amplifier at the back-off (BO) power level is given as:

$$Zm\_BO = \frac{Ao.50+Bo}{Co.50+Do} \quad (8)$$

Where:

$$\begin{bmatrix} Ao & Bo \\ Co & Do \end{bmatrix} = \begin{bmatrix} Am & Bm \\ Cm & Dm \end{bmatrix} . \begin{bmatrix} \cos\theta l & \text{j. } Z_C . \sin\theta l \\ \frac{\text{jsin}\,\theta l}{Z_C} & \cos\theta l \end{bmatrix} \quad (9)$$

At full power level, a relationship is first established between the current $I_{2m}$ and $I_{2a}$ in Figure 1. Knowing that the voltage $V_2$ is the voltage across the impedance $Z_{CN}$ at the common node through which the currents $I_{2m}$ and $I_{2a}$ flows.

$$V_2 = -Z_{CN}(I_{2m} + I_{2a}) \quad (10)$$

The main amplifier current is written as:

$$I_{1m} = -Cm.Z_{CN}(I_{2m} + I_{2a}) - Dm.I_{2m} \quad (11)$$

Additionally, the ratio of the auxiliary amplifier current to the main amplifier current for the conventional DPA is given by:

$$r = \frac{I_{1a}}{I_{1m}} = -\frac{I_{2a}}{I_{1m}} \quad (12)$$

From equations (11) and (12), we obtained:

$$\frac{I_{2a}}{I_{2m}} = \frac{-r.(Z_{CN}.Cm+Dm)}{r.Z_{CN}.Cm-1} \quad (13)$$

The impedance presented at the output of the matching quadripole at the main amplifier path, i.e. in the plane of $Z_{CN}$, is written as:

$$Zm_{CN} = -\frac{V_2}{I_{2m}} = Z_{CN}.(1 + \frac{I_{2a}}{I_{2m}}) \quad (14)$$

Thus, equation (14) makes it possible to calculate the impedance Zm seen by the main amplifier at full power (FP) and is therefore given as:

$$Zm = \frac{Am.Zm_{CN}+Bm}{Cm.Zm_{CN}+Dm} \quad (15)$$

The impedance presented at the auxiliary amplifier path, i.e. in the plane of $Z_{CN}$, is written as:

$$Za = -\frac{V_2}{I_{2a}} = Z_{CN}.(1 + \frac{I_{2m}}{I_{2a}}) \quad (16)$$

The above equations (14) to (16) are used to calculate the impedance presented to the drain of each transistor versus frequency for different current ratio r.

**Frequency behaviour of the inverted Doherty power amplifier**

Figure 3 illustrates a two-stage inverted Doherty power amplifier. This design enhances the amplifier's bandwidth at backoff power and full-power levels compared to the conventional DPA case of Figure 1.

The inverted Doherty amplifier uses two impedance transformation networks, which results in a 180° phase shift in the auxiliary amplifier path. The main amplifier always requires a quarter-wave transmission line at its input for phase compensation (Hanhui, L., et al., 2024; Chao, M., 2023; Meng, L., et al., 2020). This Doherty amplifier's architecture is called "inverted" because the delay line is placed at the input to the main amplifier instead of the auxiliary amplifier. Furthermore, the quarter-wave (λ/4) transmission lines Zc1 and Zc2 can absorb the output parasitic capacitances of the transistors, and the inverted DPA architecture allows more parameter adjustment than the conventional structure. At the back-off power level, the double λ/4 transmission lines made up of Zc2 and Zc3 improves the matching bandwidth of the auxiliary amplifier. The auxiliary amplifier path acts as a stub restoring impedance to the common node at frequencies around the central frequency fo, so that it can be exploited to improve the bandwidth.

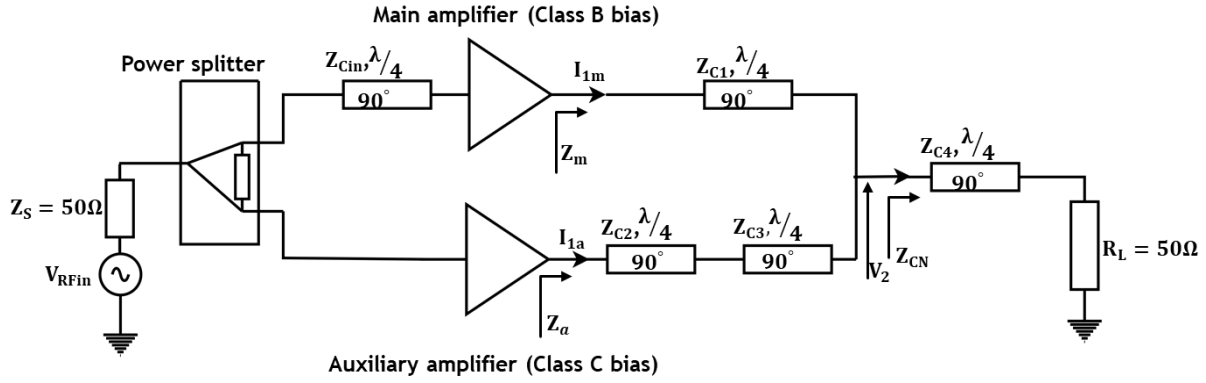


Figure 3: The Inverted DPA

**Equations for describing the frequency behaviour of the inverted DPA**

To study the frequency behaviour of the inverted DPA, the quarter-wave transmission lines at the output of the main amplifier and the two-quarter-wave transmission lines at the output of the auxiliary amplifier were also modelled in the form of the ABCD transmission matrix.

To analyse the inverted DPA and derive its design equations, we represent it using a simplified circuit with specific notations. Please refer to Figure 4 below.

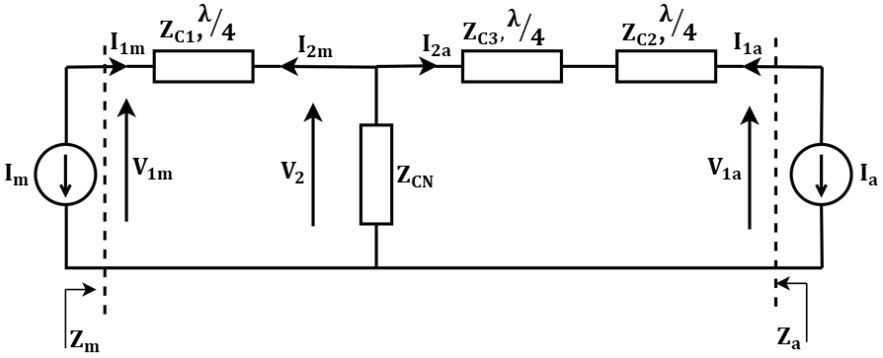


Figure 4: Equivalent circuit diagram of the proposed inverted DPA

Assuming the following expression for the ratio of the current $I_{1a}$ at the output of the auxiliary amplifier to the current $I_{1m}$ of the main amplifier of the inverted DPA:

$$r = \frac{I_{1a}}{I_{1m}} = |r|.e^{j\Delta\phi} \quad (17)$$

In contrast to the conventional DPA case, here, the current $I_{1m}$ lags $I_{1a}$ by a phase difference of $\Delta\phi = \frac{\pi}{2}$ at centre frequency $f_o$, and equation (17) now becomes:

$$r = \frac{I_{1a}}{I_{1m}} = j.|r| \quad (18)$$

The resulting expression for cascading the two quarter-wave transmission lines at the output of the auxiliary amplifier shown in Figures 3 and 4 which was modelled in the form of transmission matrix having characteristic impedances Zc3 and Zc2 at a fundamental frequency $f_o$ is written as:

$$[Z_{23}] = \begin{bmatrix} -\frac{Z_{c2}}{Z_{c3}} & 0 \\ 0 & -\frac{Z_{c3}}{Z_{c2}} \end{bmatrix} \quad (19)$$

Furthermore, the equations relating the parameters at the terminal ends of the quarter-wave transmission lines in Figure 4 are then given as follows:

$$\begin{cases} V_2 = -Z_{CN}(I_{2m} + I_{2a}) \\ V_{1m} = -j.Z_{c1}.I_{2m} \\ I_{1m} = -\frac{j.V_2}{Z_{c1}} \\ V_{1a} = -\frac{Z_{c2}}{Z_{c3}}V_2 \\ I_{1a} = \frac{Z_{c3}}{Z_{c2}}I_{2a} \end{cases} \quad (20)$$

From these equations, the impedance seen by each current source of the inverted DPA is established as:

$$\begin{cases} Zm = \frac{V_{1m}}{I_{1m}} = \frac{Z_{c1}^2}{Z_{CN}} - \frac{Z_{c1}.Z_{c2}}{Z_{c3}}.|r| \\ Za = \frac{V_{1a}}{I_{1a}} = \frac{Z_{c1}.Z_{c2}}{Z_{c3}}.\frac{1}{|r|} \end{cases} \quad (21)$$

From equation (21), we can deduce the relationship between the characteristic impedances and optimum load resistor Ropt of the GaN transistor as:

$$\frac{Z_{c1}.Z_{c2}}{Z_{c3}} = Ropt \quad (22)$$

Then, by substituting the impedance $Zm$ in equation (21) with $Ropt$, the expression for the characteristic impedance at the output of the main amplifier becomes:

$$Z_{c1} = \sqrt{Z_{CN}.(1+|r|).Ropt} \quad (23)$$

To compute the values of the impedances $Z_{c2}$ and $Z_{c3}$, it is necessary to determine the expression for the impedance $Z'_{CN}$ seen by the auxiliary amplifier at the common node path. Thus, the expression for this impedance is written as:

$$Z'_{CN} = -\frac{V_2}{I_{2a}} = Z_{CN}.(1 + \frac{I_{2a}}{I_{2m}}) \quad (24)$$

Where:

$$\frac{I_{2a}}{I_{2m}} = \frac{V_{1m}}{I_{1a}}.\frac{Z_{c3}}{-j.Z_{c1}.Z_{c2}} \quad (25)$$

And,

$$\frac{V_{1m}}{I_{1a}} = \frac{V_{1m}}{j.|r|.I_{1m}} = \frac{Zm}{j.|r|} \quad (26)$$

Using equations (25) and (23), the expression for $Z'_{CN}$ is written as:

$$Z'_{CN} = \frac{Z_{c1}.Z_{c3}}{Z_{c2}}.\frac{1}{|r|} \quad (27)$$

By using equations (20) and (23), the expression for $Z'_{CN}$ is further written as:

$$Z'_{CN} = Z_{CN}.\frac{1+|r|}{|r|} \quad (28)$$

The transmission lines with the characteristic impedances $Z_{c2}$ and $Z_{c3}$ are used to transform the impedance $Z'_{CN}$ at the common node to Ropt/($|r|$) presented to the output of the auxiliary amplifier. This can be done by calculating the intermediate resistance $R_{int}$ between the two transmission lines using the following formula:

$$R_{int} = \sqrt{Z_{CN}.\frac{1+|r|}{|r|}.\frac{Ropt}{|r|}} \quad (29)$$

We then have:

$$Z_{c2} = \sqrt{\frac{Ropt}{|r|}.R_{int}} \quad (30)$$

$$Z_{c3} = \sqrt{Z_{CN}.\frac{1+|r|}{|r|}.R_{int}} \quad (31)$$

Figure 5 shows the simplified version of the inverted DPA, which will be used to study the frequency behaviour. The quarter-wave transmission lines connected at the output of both amplifiers are synthesized by the ABCD parameters in the transmission matrix.

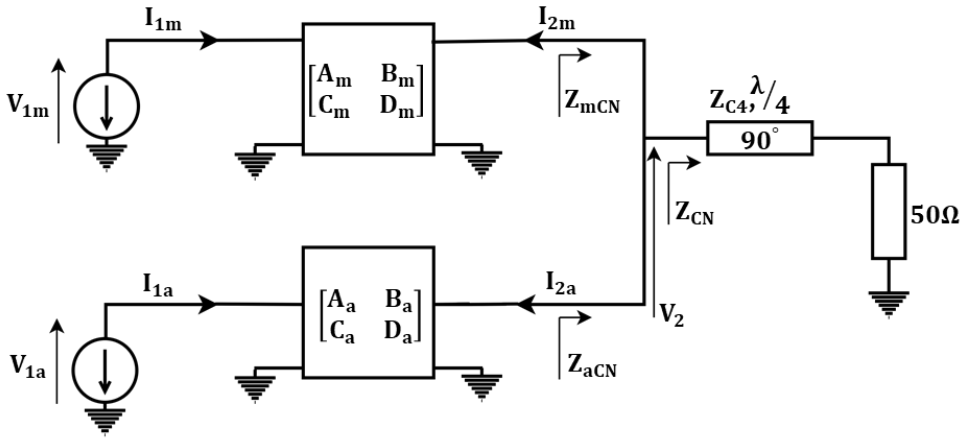


Figure 5: The simplified version of the proposed inverted DPA

To start, we need to establish a general relationship between the currents $I_{2a}$ and $I_{2m}$. To accomplish this, we will provide the equations for the currents $I_{1a}$ and $I_{1m}$ as (Eric Kerherve, 2005; Mingzhe et al., 2020; W.C. Edmund Neo et al., 2007; James et al., 2018):

$$\begin{cases} I_{1m} = -Cm.Z_{CN}(I_{2m}+I_{2a}) - Dm.I_{2m} \\ I_{1a} = -Ca.Z_{CN}(I_{2m}+I_{2a}) - Da.I_{2a} \end{cases} \quad (32)$$

By taking the ratio of the currents $\frac{I_{1a}}{I_{1m}}$, we obtain:

$$\frac{I_{2m}}{I_{2a}} = \frac{Z_{CN}.Ca - r.(Z_{CN}.Cm+Dm)}{r.Z_{CN}.Cm - Z_{CN}.Ca - Da} \quad (33)$$

The expressions for the impedance presented to the output of the matching quadripoles in Figure 5 for the main and the auxiliary amplifier's path are written as:

$$\begin{cases} Zm_{CN} = -\frac{V_2}{I_{2m}} = Z_{CN}.(1+\frac{I_{2a}}{I_{2m}}) \\ Za_{CN} = -\frac{V_2}{I_{2a}} = Z_{CN}.(1+\frac{I_{2m}}{I_{2a}}) \end{cases} \quad (34)$$

Thus, these equations can be used to calculate the impedances seen by the main and auxiliary amplifiers at full power. The equations are given by:

$$\begin{cases} Zm\_FP = \frac{Am.Zm_{CN}-Bm}{Cm.Zm_{CN}-Dm} \\ Za\_FP = \frac{Aa.Za_{CN}-Ba}{Ca.Za_{CN}-Da} \end{cases} \quad (35)$$

At the back-off power level, the auxiliary amplifier is turned off, i.e., current $I_{1a}$=0 or r=0, then, the current ratio expression of equation 33 now becomes:

$$\frac{I_{2m}}{I_{2a}} = \frac{Z_{CN}.Ca}{-Z_{CN}.Ca - Da} \quad (36)$$

From the current ratio expression of equation 33, the impedance presented at the output of the main amplifier at back-off power can be determined.

For a symmetrical two-stage inverted DPA circuit, the two transistors deliver an equal amount of current at full-power level (|r|=1). The optimum load impedance of the GaN transistor is Ropt=36 Ω, and at back-off power, the optimal drain resistance for the main amplifier is 2. Ropt=72 Ω.

When $|r| = 1$, the design equations for the inverted DPA network parameters becomes (Eric Kerherve, 2005; Mingzhe et al., 2020; W.C. Edmund Neo et al., 2007; James et al., 2018):

$$\begin{cases} Z_{c1} = \sqrt{2.Z_{CN}.Ropt} \\ R_{int} = \sqrt{2.Z_{CN}.Ropt} \\ Z_{c2} = \sqrt{Ropt.R_{int}} \\ Z_{c3} = \sqrt{2.Z_{CN}.R_{int}} \\ Z_{c4} = \sqrt{50.Z_{CN}} \end{cases} \quad (37)$$

From this set of equations, it can be observed that the characteristic impedances of the quarter-wave transmission lines depend on the choice of the common node impedance $Z_{CN}$. This provides additional adjustment possibilities compared to the conventional DPA architecture. Furthermore, it is also possible to adjust the intermediate impedance $R_{int}$, between the two quarter-wave transmission lines at the output of the auxiliary amplifier as well as the phase slope parameter, $\gamma$.

The 'fmincon' Optimization solver:

This solver is used to find the minimum of a constrained multivariable function. It is a nonlinear programming solver used to locate the minimum of functions specified in the following form:

min $x$f(x) such that: A*x ≤ b, Aeq*x = beq (Linear constraints)

C(x) ≤ 0, Ceq(x) = 0 (nonlinear constraints)

Lb ≤ x ≤ Ub (bounds)

While b and beq are vectors, A and Aeq are matrices. Functions that return vector values are given by C(x) and Ceq(x), while f(x) is a function that returns a scalar value. The fmincon optimization solver has five different algorithms: the interior point algorithm, which is the default algorithm of the fmincon solver; active-set; sequential quadratic programming (Sqp); Sqp-legacy; and trust-region-reflective algorithms. The fmincon solver is applicable when the constraint and the objective function to be minimized are continuous (Lagarias, J.C., et al., 1998). In addition to this, the objective and constraint functions must be real values and not complex. It is highly recommended to always start with the default algorithm (Interior-Point) when applying the fmincon solver to find the minimum of a constrained function. However, when the size of the objective function to be optimized is in the range of small and medium, the Sqp or active-set algorithm is used to obtain more speed. Both the fmincon optimization solver (SQP algorithm) and the fmincon solver (active set algorithm) are robust to variation of initial values and converge faster (fr.mathworks.com, 2022; The Mathworks, Inc., 2018; The Mathworks, 2001).

**Improving the bandwidth of an inverted DPA using the optimization method**

***The optimization process***

It is possible to optimise the bandwidth of an inverted DPA by adjusting the impedance $Z_{CN}$ seen at the common node, the intermediate impedance $R_{int}$ between the two quarter-wave transmission lines at the output of the auxiliary amplifier, and by varying the input phase slope difference between the main and auxiliary currents as a function of the phase slope parameter $\gamma$.

The optimization parameters focus on the characteristic impedances (Zc1, Zc2, Zc3, and Zc4) as well as the phase slope parameter $\gamma$.
The following are the input variables to the optimization function:
• The frequency range of the optimization = 2 GHz to 3 GHz
• The main amplifier optimum load impedance, Ropt= 36 $\Omega$
• The main amplifier output parasitic capacitance, Cd = 1.3 pF
• The initial value of the phase slope parameter, $\gamma$ = 2
• The magnitude of the current ratio is |r|=1 for symmetrical Doherty transistors
• The common node resistance value is given as $Z_{CN}$ = Ropt= 36 $\Omega$
• Subsequently, the calculation of the following initial values of the optimization parameters
(Zc1, Zc2, Zc3, and Zc4) is carried out using equations (37)
• Then, the MATLAB fmincon optimization solver using the sequential quadratic programming
(Sqp) algorithm is invoked on the optimization objective function.
• The objective function of the optimization program is given by the summation of the maximum values of the voltage standing wave ratio for the main amplifier at back-off power, main amplifier and the auxiliary amplifier at full power.
The fmincon solver otherwise referred to as constrained linear optimization is used to find the constrained minimum of an objective function starting from an initial value of $x_0$. It is described by the following MATLAB syntax:
[x, fval, exit flag, output] =fmincon (objfun, $x_0$, A, b, Aeq, beq, lb, ub, nonlcon, options).
Where, A = b= Aeq = beq= nonlcon = [] were choosing to be empty matrices since we are not imposing any inequality or equality constraints on the optimization problem.
The lower (lb) and upper (ub) bound values of the optimization variables are defined so that the optimization solution falls in between the two boundaries. Thus, the lower and upper bound values for the optimization variable are given as:
lb= [10Ω; 10Ω; 10Ω; 10Ω; 0.5], ub= [50Ω; 50Ω; 100Ω; 70Ω; 6].
The options argument for the fmincon solver with Sequential Quadratic Programming (SQP) algorithm is given as:
Options = optimoptions ('fmincon', 'Algorithm', 'Sqp', 'Tolx', 1e-9, 'StepTolerance', 1e-16, 'MaxFunctionEvaluations', 5000).

## RESULTS AND DISCUSSION

### Analyzing the frequency behaviour of the conventional DPA

The design of the DPA aims to achieve a VSWR of a maximum value of 1.2, which corresponds to a reflection coefficient value of less than -20.8 dB over the widest possible frequency bands, with a fractional bandwidth of 40%, spanning 2–3 GHz.
The VSWR are calculated at back-off power for the main amplifier and full power for the main and auxiliary amplifiers. Both transistors in the DPA circuit are presumed to be identical in size (i.e., |r|=1) and deliver an equal amount of current at a high-power level. When operating at full power, each transistor is presented with an optimum impedance of Ropt=36 Ω at the output. Conversely, at the back-off power level, the main amplifier's output is presented with an optimal impedance of 2.Ropt=72Ω.
Consequently, Table 1 summarises the conventional DPA circuit parameter values designed at center frequency of 2.5 GHz using quarter-wave transmission lines modelled in the form of transmission matrices.

**Table 1: The conventional DPA circuit parameter values at centre frequency of 2.5 GHz**

| Current ratio | Phase slope parameter | Opt. load at Full Power | $Z_c$ main ¼ wave | Z commun node | $Z_c$ output ¼ wave |
|---|---|---|---|---|---|
| $\|r\|$ | $\gamma$ | Ropt | $Z_{C1} = Ropt$ | $Z_{CN} = \frac{Ropt}{1+\|r\|}$ | $Z_{C2} = \sqrt{50.Z_{CN}}$ |
| 1 | 2 | 36 Ω | 36 Ω | 18 Ω | 30 Ω |

However, it should be noted that the main amplifier determines the bandwidth limit of the DPA.
Figure 6 shows the frequency response of the conventional DPA in terms of the VSWR for the main amplifier at 6 dB backoff power and for the main and auxiliary amplifiers at Full power. This result represents a classical case with a perfect matching at a center frequency of $f_o$=2.5 GHz. Then a degradation in the matching increases as the frequency moves away from the central point. The reason for the worst VSWR at the band edges is due to impedance mismatch as the frequency moves away from the center frequency of 2.5 GHz. The maximum VSWR value is worst at 40% relative bandwidth (i.e., between $f_o$ of 2 GHz or 3 GHz). However, operation of the DPA will be limited in bandwidth at Back-Off power with a maximum VSWR value of $VSWR_{max}$=2.1.

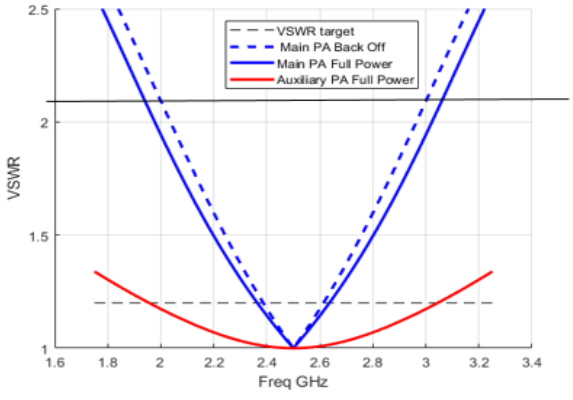


Figure 6: Frequency response result of the VSWR with Table 1 element values

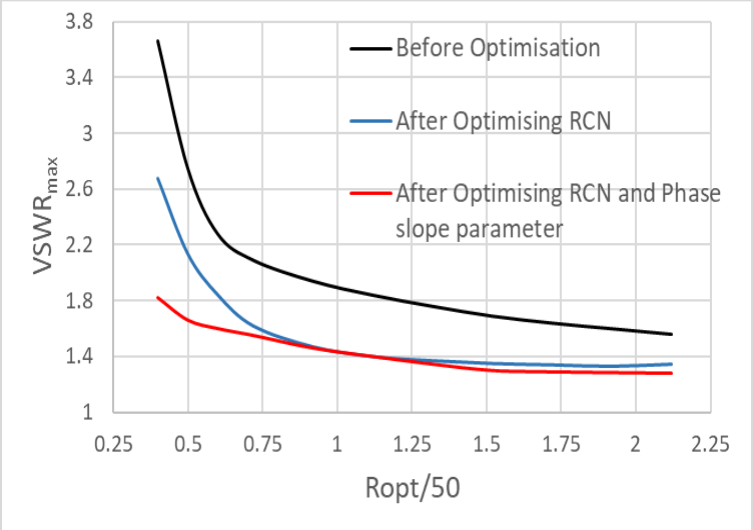


Figure 7: Maximum VSWR at 40% fractional bandwidth as a function of normalised Ropt

Figure 7 shows the plot of the maximum $VSWR_{max}$ at 40% fractional bandwidth as a function of normalised optimum load resistance of the GaN transistor (Ropt/50). The simulated frequency response of the symmetrical conventional DPA at 40% fractional bandwidth in terms of the VSWR for the main amplifier at 6 dB backoff power and the main and auxiliary amplifiers at Full power are compared at different values of Ropt. The black curve shows the frequency response of the conventional DPA using the amplifier's network parameters calculated values at a centre frequency of 2.5 GHz. To improve the bandwidth of the conventional DPA, the common node impedance ($Z_{CN}$) was optimized using fmincon MATLAB optimization solver with SQP algorithm at a centre frequency of 2.5 GHz. The result in blue curve shows a slight improvement of the VSWRmax at the band edge, even though the amplifier is no longer perfectly matched at centre frequency.

To further improve the bandwidth of the conventional DPA, both the common node impedance $Z_{CN}$ and phase slope parameter ($\gamma$) values between the main and auxiliary amplifiers were optimized. In this case, as depicted by red curve, an improvement in VSWRmax can be seen mainly at low Ropt/50 ratios, corresponding to the highest power levels. This result shows that the VSWR value of the DPA at the band edge improves as the optimum load resistance increases. Thus, at higher Ropt value of 100 Ω corresponding to a normalised Ropt value of 2, the VSWR value is around 1.3.

Thus, for Conventional DPA, the bandwidth at the edges of the VSWR (2 GHz or 3 GHz) for the main amplifier at backoff and full power, as well as that of the auxiliary amplifier at full power slightly improved upon optimizing its $Z_{CN}$ and phase slope parameter values.

**Analyzing the frequency behaviour of the inverted DPA**

Table 2 summarises the values of the circuit parameters of the inverted DPA at two common node impedance value of $Z_{CN}$ = Ropt/2=18 Ω, (like the conventional DPA case) and $Z_{CN}$ = Ropt=36 Ω.

**Table 2: The network parameter values of the inverted DPA**

| | Current ratio | Z common node | Phase slope param. | Opt. load at Full Power | $Z_{c1}$ main ¼ wave | R inter-mediate | $Z_{c2}$ Aux. ¼ wave | $Z_{c3}$ Aux. ¼ wave | $Z_{c4}$ output ¼ wave |
|---|---|---|---|---|---|---|---|---|---|
| | $\|r\|$ | $Z_{CN}$ | $\gamma$ | Ropt | $Z_{C1}$ | *Rint* | $Z_{c2}$ | $Z_{c3}$ | $Z_{C4}$ |
| Case 1 | 1 | 18 Ω | 2 | 36 Ω | 36 Ω | 36 Ω | 36 Ω | 36 Ω | 30 Ω |
| Case 2 | 1 | 36 Ω | 2 | 36 Ω | 51 Ω | 51 Ω | 42.8 Ω | 60.5 Ω | 42.4 Ω |

Figures 8 and 9 show the VSWR performance of the main amplifier at a threshold value of 1.2 during back-off power, as well as the performance of both the main and auxiliary amplifiers at full power levels. The calculations were performed at a common node impedance value of $Z_{CN}$ = Ropt/2 = 18 Ω and $Z_{CN}$ = Ropt = 36 Ω. The results indicate that the frequency response for case 1 is similar to that of the conventional Doherty power amplifier architecture of Figure 6, while case 2 of Figure 9 demonstrates improved performance over case 1, as the VSWR at the band edges for the main amplifier at backoff power and for the main and auxiliary amplifiers at full power has significantly improved as their VSWR values fall below the threshold value of 1.2.

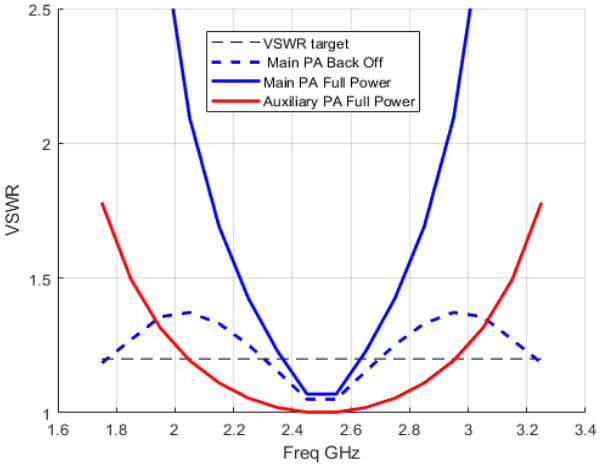


Figure 8: Frequency response of the VSWR for case 1 of Table 2

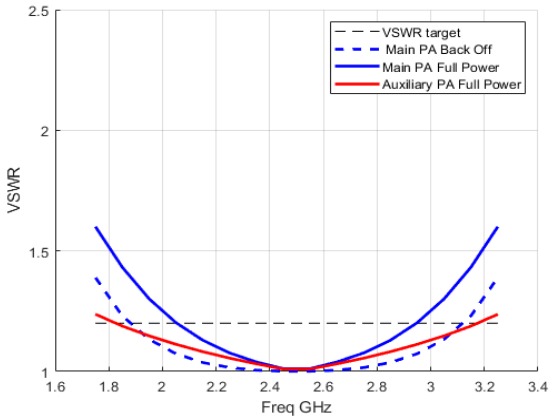


Figure 9: Frequency response of the VSWR for case 2 of Table 2

Figure 10 illustrates the impact of adjusting common node impedance $Z_{CN}$ on the maximum VSWR values at a 40% fractional bandwidth for both the main and auxiliary amplifiers, considering the main amplifier either at back-off or at full power, and for two different Ropt values. In this section, a sweep of $Z_{CN}$ = $R_{CN}$ is conducted, and the characteristic impedances of the transmission lines for the inverted DPA are updated for each value of $R_{CN}$. Additionally, the VSWR values for the inverted DPA are calculated at the edges of the targeted bandwidth, specifically at 2 GHz or 3 GHz.

As shown in Figure 10, the plot of the VSWR for the inverted DPA against the common node resistance $R_{CN}$ confirms the significant impact of both the choice of common node resistance and the optimal load resistance Ropt on frequency response performance. For the two cases of Ropt values, the frequency response of the VSWR for the main amplifier at backoff power, as well as for both the main and auxiliary amplifiers at full power at the band edges, improves as the common node resistance increases. However, when Ropt is set to 36 Ω, performance is noticeably better, with the VSWR for the main amplifier at backoff power and for the main and auxiliary amplifiers at full power at the band edge remaining below the threshold value of 1.2. At this point, the optimal value for the common node resistance is determined to be $R_{CN}$=36 Ω. Therefore, modifying the $Z_{CN}$ value should be considered when optimizing bandwidth.

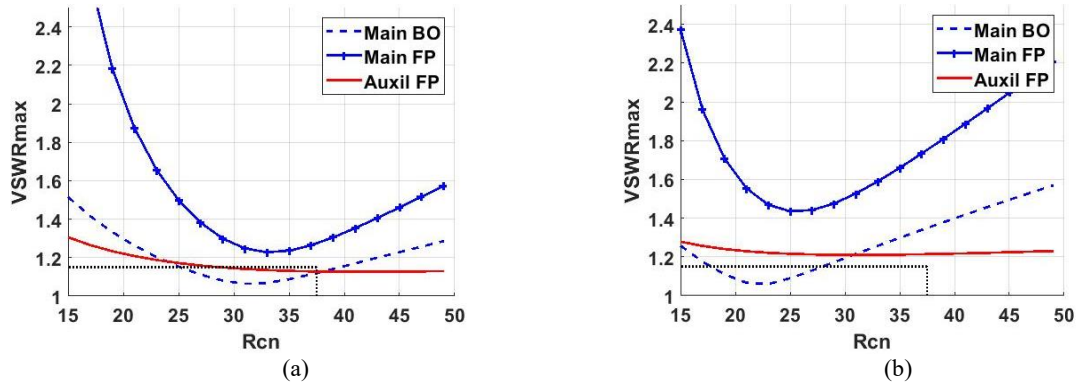


Figure 10: Effect of $R_{CN}$ on the maximum $VSWR_{max}$ of each amplifier for: a) Ropt=36 Ω, b) Ropt = 18 Ω

Figure 11 illustrates the results of optimizing the inverted DPA architecture at various Ropt values. This process begins by adjusting $R_{CN}$ alone, followed by simultaneous adjustments of $R_{CN}$ and the phase slope (as shown in the red plot), and finally includes adjustments to the four characteristic impedances along with the phase slope (depicted in the black plot). Modifying the phase slope enhances the performance of the amplifiers within the relevant frequency band. Further improvements can be achieved by also fine-tuning the four characteristic impedances. The MATLAB-based Sequential Quadratic Programming (SQP) method was used to carry out the optimization.

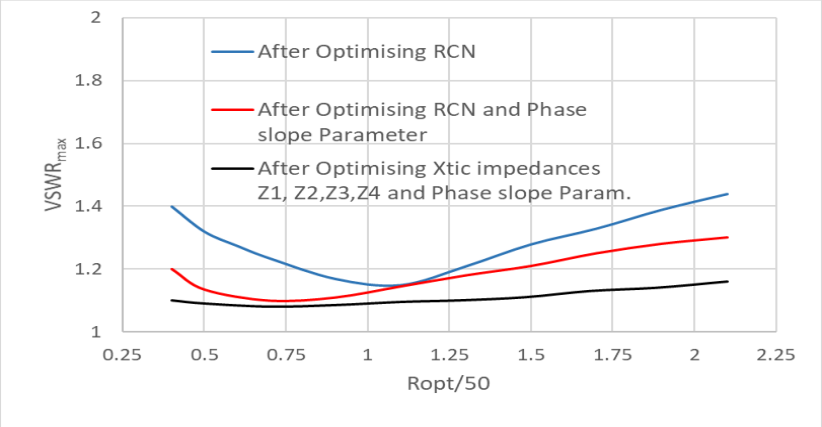


Figure 11: Maximum VSWRmax at 40% bandwidth as a function of normalised Ropt for Inverted DPA

The advantage of these adjustments is that the Voltage Standing Wave Ratio (VSWR) for each amplifier can be maintained at low values, below 1.2, even at low values of Ropt corresponding to high amplification powers. Figure 12 illustrates the variations in VSWR at the output of each amplifier for an Ropt value of 36 Ω. The simulated frequency response of the symmetrical inverted Distributed Power Amplifiers (DPAs) shown in Figure 12, in terms of VSWR at a threshold value of 1.2, was analyzed for the main amplifier at 6 dB back-off power, as well as for both the main and auxiliary amplifiers at full power. This analysis involved adjusting the common node impedance ($R_{CN}$), intermediate resistance ($R_{int}$), as well as optimizing the four characteristic impedances, and the phase slope parameter using the MATLAB optimization solver with the Sequential Quadratic Programming (SQP) algorithm. The results indicate that the VSWR value for the main amplifier at both full and back-off power, as well as for the auxiliary amplifier at full power, is approximately 1.1 which remains below the threshold value of 1.2 across the desired frequency range of 2 GHz to 3 GHz, thereby achieving the 40% fractional bandwidth.

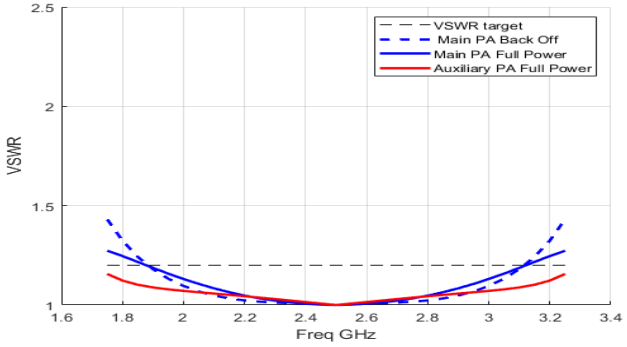


Figure 12: Frequency response of the optimised VSWR

In summary, the results of both the conventional and inverted DPAs showed that adjusting the DPAs phase slopes and output network parameters can enhance the amplifier's operating bandwidth. However, the improvement in bandwidth for the inverted DPA architecture is higher than the conventional DPA type. Moreover, the inverted DPA topology offers the potential to adjust various circuit parameters to control its bandwidth limits. Notably, the slope of the phase variation between the main and auxiliary amplifier currents, as highlighted in the work of (Manuel et al., 2023), is a crucial parameter for adjusting and controlling the bandwidth limit.

## CONCLUSION

This paper introduces the frequency behaviour of two-stage Doherty power amplifier architectures: the conventional Doherty amplifier and the inverted Doherty amplifier. Through theoretical derivation and optimization, the study shows that the inverted Doherty power amplifier delivers better bandwidth performance compared to the conventional design. This improvement is observed at both full and back-off output power levels across the 2–3 GHz frequency range. Further analysis indicates that optimizing the input phase slope and the impedances of the four quarter-wave transmission lines (Zc1, Zc2, Zc3, and Zc4) significantly enhances bandwidth. This analysis utilizes an NXP GaN-based FET transistor model to validate the theoretical

findings. The inverted Doherty amplifier achieved a 40% fractional bandwidth within the 2–3 GHz range, in contrast to the 8% fractional bandwidth of the conventional DPA, at a Voltage Standing Wave Ratio (VSWR) threshold of 1.2, outperforming the conventional design due to greater parameter flexibility.

While the inverted DPA offers improved bandwidth, its implementation complexity and potential impact on power efficiency should be considered in practical designs. Additionally, the results presented are based on theoretical analysis and MATLAB simulations; experimental validation is recommended for future work. These findings are particularly relevant for 5G base station applications, where wider bandwidth is crucial for high-data-rate transmission. However, while the inverted DPA offers superior bandwidth, the conventional DPA remains advantageous in applications requiring simpler design and implementation.

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