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HIGH EFFICIENT BROADBAND CLASS-E POWER AMPLIFIER DESIGN USING SYNTHESIZED LOW-PASS MATCHING NETWORKS

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ABSTRACT
High-efficiency broadband Class-E power amplifiers (PAs) using high-order low-pass filter prototype is presented. A Gallium Nitride GaN transistor was used and characterized to prescribe the optimal output impedance for the broadband Class-E operation. A sixth order low-pass filter matching network was designed and implemented for the output matching. While the output provides optimized fundamental and harmonic impedances within an octave bandwidth. The simulated results show that an optimal band of operation was realized from 1.2GHz to 2GHz with an efficiency measured from 80% to 89%. An overall power amplifier bandwidth of 0.9GHz to 2.2GHz was measured between 10W to 20W output power with gain of 10dB to 13dB and efficiency was found to be around 63% to 89% throughout the band.

Keywords: *Broadband, Class-E, GaN transistor, High efficiency, High power, Low-pass matching network, Power amplifier (PA), Synthesis*

INTRODUCTION

High power and high efficiency power amplifiers (PAs) are very important in modern wireless communication systems, especially those in base-stations, to achieve low-cost and highly reliable transmitters. High-efficiency PAs are commonly realized using switch-mode topologies, such as Class-D, Class-E, and Class-F, or harmonic-tuned circuitries, like Class-F and Class-J (Cripps, 2006). These highly efficient PAs usually require a high saturation level of the device and accurate harmonic engineering, leading to bandwidth restrictions in their frequency response (Adah and Zirath, 2003, Saad *et al*. 2009). Never the less, future communication systems, e.g.,Wi Max and LTE, would require wider bandwidths not only for the coverage of multiple frequency bands but also to increase effective bandwidths of the signal up to 100MHz. The military wireless systems require even wider bandwidths, typically above an octave. The distributed amplifier (DA) is the common solution for wideband amplification (Entesari *et al*. 2009). However, this approach requires multiple devices, which results in a low overall efficiency. Another possible solution based on the optimization of the fundamental harmonic impedance has been presented in (Colantonio *et al*. 2008) and (Sayed and Tanany, 2009), achieving multi-octave bandwidths. However, significant higher order harmonics remain in such designs, leading to relatively low efficiencies (Colantonio *et al*. 2008 and Tanany and Sayed, 2009 obtained 50%, 20% with harmonic distortion). Several design techniques have been proposed and demonstrated with an optimization of bandwidth and efficiency (Wright *et al*. 2009), (Saad *et al*. 2010). Therefore, the comparison features of these PAs were summarized in Table 1. It is important to note that the matching network topologies used in those designs are equivalent to low-pass prototypes with an order $n \leq 4$. Herein, a model design of high efficient class-E power amplifier using synthesized low-pass matching networks for broadband application is proposed.

THEORETICAL BACKGROUND

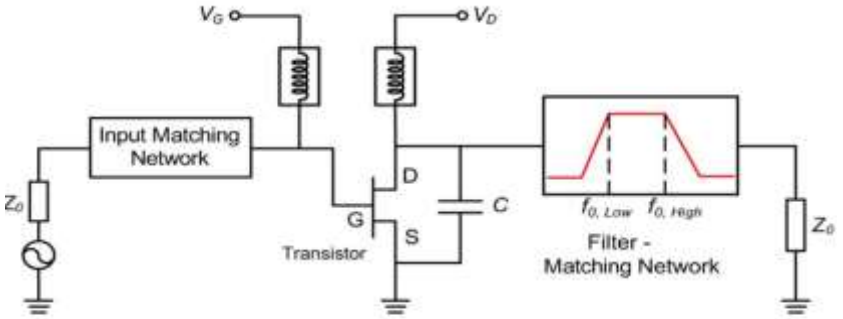

Figure1: Broadband Class-E PA topology

Here, the transistor is considered to act as a switch with capacitor C_I connected in parallell. If the transistor switch is turn on, the current flows entirely through the switch drain and source, therefore the voltage is zero (Mader *et al*.,1998). The current can be expressed as:

$$I_{sw}(t) = Idc[1 + a\sin(wt + \emptyset)] \quad (1)$$

When the switch is turned off, the current flow entirely into the capacitor which is charged simultaneously. During this off state interval, the voltage on this parallel capacitor is given by:

$$V_{sw}(t) = \frac{1}{C_I}\int_o^t I_{sw}\,(t^I)\,dt^I$$

$$= \frac{Idc}{WC_I}\,[1 + a(\cos(wt + \emptyset)] \quad (2)$$

There are two boundary conditions for the ideal class E operation (Ewing,1964), which are; zero voltage switching (ZVS) and zero voltage derivative switching (ZVDS) conditions.

Assume the switch is turned off at t=0 and turned on at $= \frac{T}{2}$, those two conditions are given by:

$$V_{sw}\,(t = 0\,) = 0$$

$$\frac{dV_{sw}}{dt}\,(\,t = \frac{T}{2}\,) = 0 \quad (3)$$

Where T denotes the time period of one class E duty cycle. The ZVS condition prevents simultaneous non zero voltage and current across the switch device while the ZVDS enforce the current to start flowing after the voltage has reached zero .

The value of *a* and ∅ can be determined uniquely by applying these two constraints leading to; where *a* is the amplitude of the output voltage, ∅ is the phase shift between the output voltage and the input signal at the transistor gate.

$$a = \frac{\sqrt{1+\pi^2}}{4} \quad (4)$$

$$\emptyset = \arctan\frac{2}{\pi} \quad (5)$$

Consequently, there is no overlap between the transient drain current and voltage, which leads to a zero dc power dissipation and 100% drain efficiently. Using Fourier series expansion (Cipriani *et al.*, 2008) the optimal fundamental load, yielding perfect class E operation can be determined by:

$$Z_{E,f_o} = \frac{0.28}{WC_I}e^{49°} \quad (6)$$

This impedance presents inductive, which is illustrated in Fig 1. In ideal class E mode, the total current through the combined switch capacitor tank is a pure sinusoidal wave, and the harmonics are entirely due to the voltage. The ideal impedances at higher order harmonic frequencies are infinite, which is given by;

$$Z_{E,nf_o} = \infty, \quad n \geq 2 \tag{7}$$

Sokal *et al*, (1975) proposed the original design of the Class-E amplifier. They assumed ideal passive components and an ideal switching transistor. These approximations lead to the following conditions in the amplifier:

- Choke inductor current i_{LC} will be a DC signal,
- The output current $i_0$will be a perfect sinusoidal waveform, and
- The transistor will turn instantly ON and OFF with zero ON resistance and

infinite OFF resistance.

Under these conditions, if the drain voltage and the drain current are never both non-zero at the same time, then no power will be consumed by the transistor, and with ideal passives, the amplifier will operate at 100% efficiency.

From the above assumptions, the choke current and the output current can be defined as:

$$i_{LC} = I_{DC} \tag{8}$$

$$i_0 = \frac{a}{R}\sin(\omega t + \Phi) \tag{9}$$

where a is the amplitude of the output voltage, R is the output load resistance and φ is the phase shift between the output voltage and the input signal at the transistor gate. Using KCL at the drain of the transistor yields the following equation;

$$i_{LC} = i_{CP} + i_D + i_0 \tag{10}$$

Since the transistor and the parallel capacitor C_P are in parallel, when the transistor is ON, no current flows through C_P. However, when the transistor is OFF, zero can be substituted into Equation (10) for i_D with the results of Equation (9) yielding;

$$i_{CP} = 0 \quad [\text{ON}] \tag{11}$$

$$i_{CP} = I_{DC} - \frac{a}{R}\sin(\omega t + \Phi) \quad [\text{OFF}] \tag{12}$$

Substituting the results of Equation (9) into Equation (10) along with the result that i_{CP} =0 in the ON state yields the drain equations as follow;

$$I_D = I_{DC} - \frac{a}{R}\sin(\omega t + \Phi) \quad [\text{ON}] \tag{13}$$

$$I_D = 0 \qquad [\text{OFF}] \tag{14}$$

Knowing that a current flowing into a capacitor produces a voltage and knowing that the parallel capacitor voltage is the same as the drain voltage yields the following equation for the drain voltage V_{DS} (Sokal *et al*, 1975).

$$V_{DS} = \frac{1}{C_p}\int_{t=0}^{t} i_{CP}\,dt = \frac{1}{C_p}\int_{t=0}^{t}\left(I_{Dc} - \frac{a}{R}\sin(\omega t + \Phi)\right) dt$$

$$= \frac{1}{C_p}\left[I_{Dc}t + \frac{a}{WR}\cos(\omega t + \Phi) - \frac{a}{WR}\cos(\Phi)\right] \tag{15}$$

METHODOLOGY

The first step was the design of a 5:1 real to real Chebyshev low pass matching network within the desired bandwidth. Due to the difficulty in getting high-quality inductors and capacitors at the desired frequency range, the low pass matching network was implemented with all distributed elements in this work. Also, the inductors were replaced with high impedance transmission line sections, and the capacitors were replaced with low impedance open circuit stubs. The matching network topologies used in these designs are equivalent to low-pass prototypes with an order $n \leq 4$.

However, in the method of designing a broadband high-efficiency class-E PA high-order low-pass circuit topologies with the input $n \geq 8$ and output $n \geq 6$ was adopted. By way of comparison to Class-D designs, the presented Class-E power amplifier exhibits simpler circuitry and reduced sensitivity to parasitics. However, when compared to Class-F

design, it is more for giving to harmonic terminations requirements and allows for a broadband performance. The design was based on a commercially available 25-W Cree GaN HEMT device. A three-stage Chebyshev low-pass network with $n = 6$ was synthesized for the output matching, and implemented using transmission lines. Optimal fundamental second-harmonic and third-harmonic impedance terminations were provided for the transistor output over a broad bandwidth using Advance Design Circuits Software.

RESULTS AND DISCUSSION

The maximum power added efficiency achieved in this paper is about: 63% - 89% and output power is 10W to 20W for 12V power supply voltage at frequency range 0.9 to 2.2GHz. The results comparison is shown in Table 1.

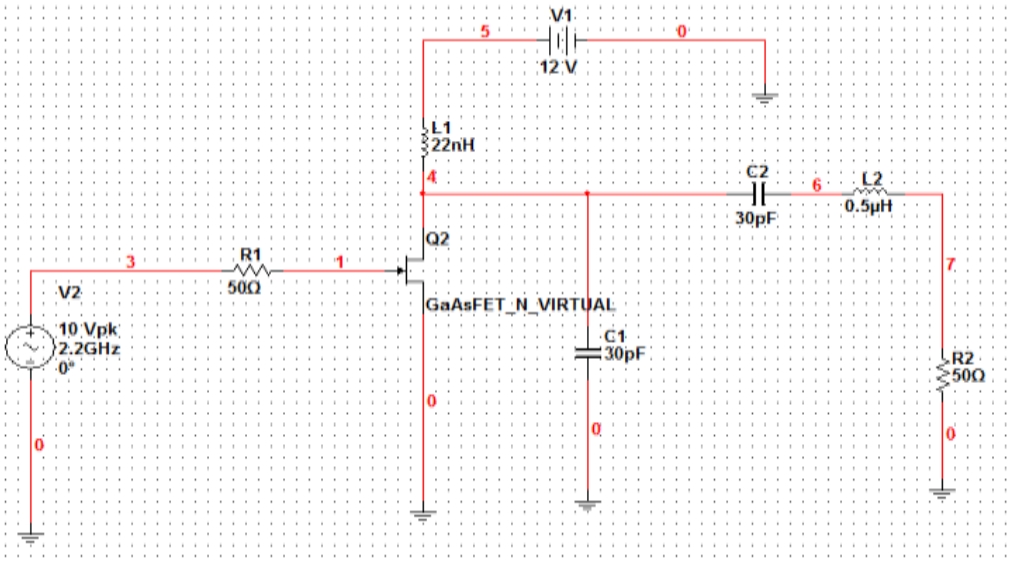

Fig. 1: Configuration of Class-E Power Amplifier

Table 1: Comparison of High Efficiency Broadband Power Amplifier

P.A. Mode	Bandwidth (GHz)	Gain (dB)	P_{OUT} (W)	Efficiency (%)	Reference
Class J	1.4 to 2.6	11 to 12	9 to 11	57 to 72	Wright *et al*., 2009
Class E	2.0 to 2.5	10 to 13	7 to 12	74 to 77	Vander *et al*. 2009
Class E	0.6 to 1.0	12 to 18	45 to 49	66 to 87	Tanany and Sayed, 2009
-	1.8 to 3.1	9 to 10	20 to 50	56 to 65	Wu *et al*., 2010
-	1.9 to 4.3	9 to 11	10 to 15	57 to 72	Saad *et al*., 2010
Class E	0.9 to 2.2	10 to 13	10 to 20	63 to 89	This work

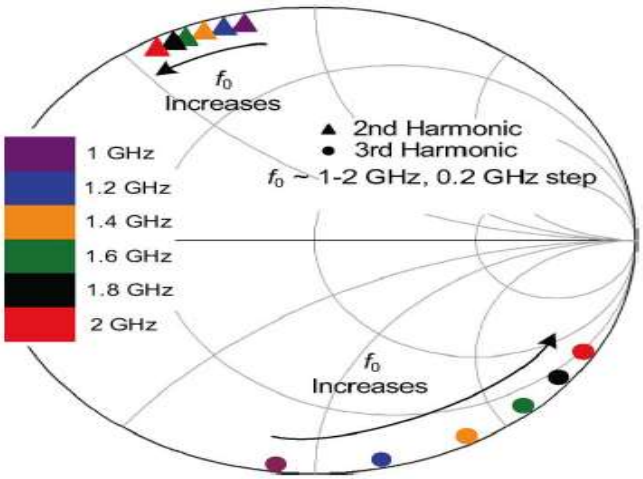

Fig. 3: Optimal impedance of the second and third harmonics

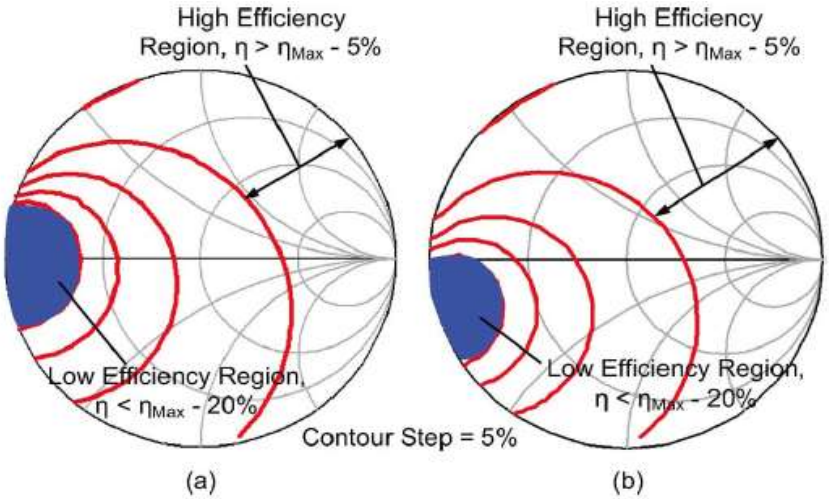

Fig. 4: Simulated load–pull contours of the second harmonic impedance: (a) at $2f_0$ = 2GHz and (b) at $2f_0$ = 4GHz.

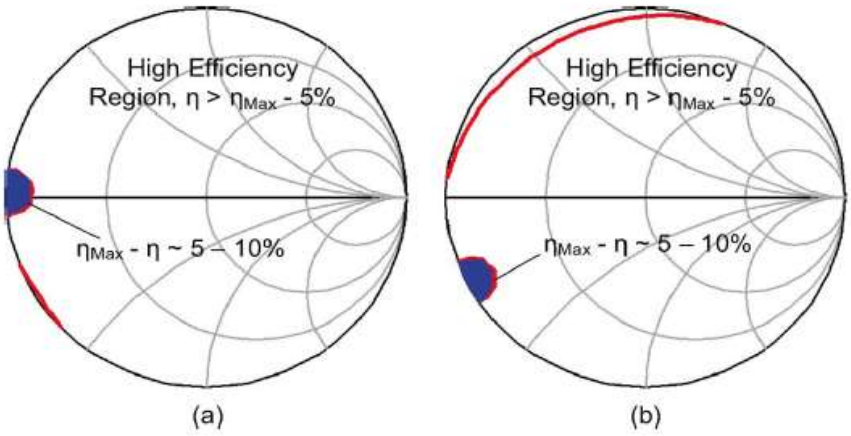

Fig. 5: Simulated load–pull contours of the second harmonic impedance: (a) at $2f_0$ = 3GHz and (b) at $2f_0$ = 6GHz.

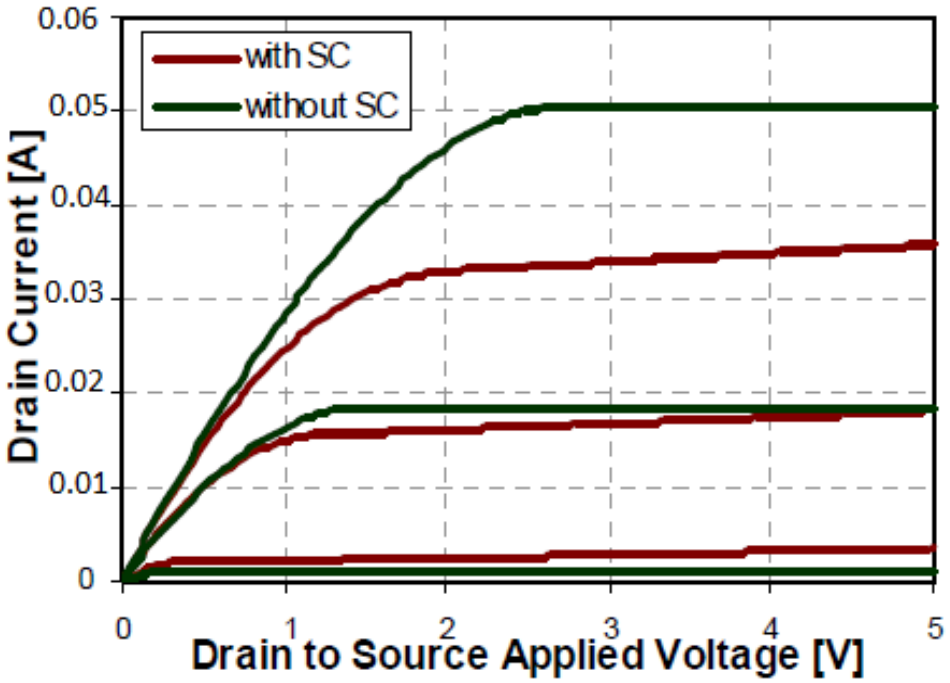

Fig. 6: IV Characteristic

DISCUSSION

This design achieves a state-of-the-art performance compared to the other published results. The load–pull simulation is carried out to provide the optimal harmonic impedances at the package plane. Figure 3 depicts the optimal impedances of second and third harmonics when frequency varies from 1 to 2GHz. The second harmonic impedance plays the most important role, it improved the efficiency of Class-E PA. Figure 4 shows the simulated load–pull contours of the second harmonic at 1 and 2GHz, indicating the tolerable region of the second harmonic impedance in which high efficiency can be achieved. Figure 5 illustrates the contours of the third harmonic at 1GHz and 2GHz. This shows that the efficiency is less sensitive at such regions. Furthermore, the simulated load–pull contours of the third harmonic impedance were found to be at 3GHz and 6GHz showing maximum efficiency drop by only 10% in the small blue regions. Also, as the second harmonic impedance of the frequency near 1GHz would be close to the fundamental matching impedance of 2GHz. Furthermore, the presented design strives for achieving optimal results between 1.2GHz to the 2-GHz region. Simulated fundamental output powers of 0.9 to 2.2GHz bands were in the range of 10 to 20W. The power gain of this broadband Class-E PA ranges from 10 to 13dB within the entire bandwidth. The second and third harmonics were also measured using the spectrum analyzer when is operating below 1.2GHz. The favourable harmonic impedances were provided by the output matching network and power amplifier efficiencies ranges of 63% to 89%.within the entire band obtained from the simulation.

CONCLUSION

The method for designing a broadband high-efficiency Class-E PA that employs high-order low-pass circuit topologies at the input $n \geq 8$ and output $n \geq 6$ was presented. Three-stage low-pass network was synthesized and implemented for the output matching of a Cree GaN transistor, which provides broadband impedance matching for both fundamental and harmonics. The broadband Class-E operation and the results were in good agreement with other works. An efficient power amplifier performance was measured across a bandwidth of 0.9 to 2.2GHz with the efficiencies of 63% to 89%. The power gain of this broad band Class-E power amplifier was in the range from 10dB to13dB within the entire bandwidth.

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